



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/632,024

07/31/2003

Gerard Chauvel

TI-35461

9347

23494

7590

07/08/2009

TEXAS INSTRUMENTS INCORPORATED

P O BOX 655474, M/S 3999

DALLAS, TX 75265

EXAMINER

SWEARINGEN, JEFFREY R

ART UNIT

PAPER NUMBER

2445

NOTIFICATION DATE

DELIVERY MODE

07/08/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No. 10/632,024	Applicant(s) CHAUVEL ET AL.	
	Examiner Jeffrey R. Swearingen	Art Unit 2445	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 26-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (US 5,867,723) in view of Boutaud et al. (US 6,334,181).

4. In regard to claim 26, Chin disclosed *a processor system comprising:*

A. first processor circuitry having a memory transaction bus, a wait signal input, and status signal inputs; Chin, Figure 3, Figure 29, column 45, lines 5-28

B. second processor circuitry having a memory transaction bus, a wait release signal output, and status signal outputs connected with the status signal inputs; Chin, Figure 3, Figure 29, column 45, lines 5-28

C. memory circuitry having first connections with the memory transaction bus of the first processor separate from second connections with the memory transaction bus of the second processor circuitry; and Chin, Figure 3

D. wait circuitry having memory transaction bus inputs connected with the memory transaction bus of the first processor circuitry and the first connections, being

Art Unit: 2445

free of any connections with the memory transaction bus of the second processor circuitry, and having a wait signal output connected with the wait signal input, and a wait release signal input connected with the wait release signal output. Chin, column 45, lines 5-28 disclosed use of a wait state system. Chin failed to disclose the wait state circuitry.

Boutard disclosed a wait state generator for use in a processor and bus system. Boutard, Figure 27. It would have been obvious to one of ordinary skill in the art at the time of invention to use the Boutard wait state circuitry with the Chin multiprocessor system in order to allow the controllers in the Chin system to synchronize properly. Chin, column 45, lines 5-28.

5. In regard to claim 27, Chin further disclosed *the first processor circuitry includes a system interrupt input, and the wait circuitry has a processor interrupt output coupled with the system interrupt input.* Chin, Figure 24, Figure 33

6. In regard to claim 28, Chin further disclosed *the first processor circuitry has a system interrupt detect output, and the wait circuitry has a system interrupt detect input coupled with the system interrupt detect output.* Chin, Figure 24, Figure 33

7. In regard to claim 29, Chin further disclosed *the first processor circuitry includes a system interrupt input, the wait circuitry has a processor interrupt output and a system interrupt detect input, and including a system interrupt controller having system interrupt output connected with the system interrupt input, a system interrupt detect output connected with the system interrupt detect input, and a processor interrupt input connected with the processor interrupt output.* Chin, Figure 24, Figure 33

8. In regard to claim 30, Chin disclosed *wait circuitry comprising:*

A. first processor interface circuitry having a wait signal output, a processor interrupt output, and memory transaction bus connections; Chin, Figure 3, Figure 29, column 45, lines 5-28

B. second processor interface circuitry having a wait release signal input and being free of any connections with any memory transaction bus of the second processor circuitry; Chin, Figure 3, Figure 29, column 45, lines 5-28

C. system interrupt interface circuitry having a system interrupt detect input;

D. decode logic circuitry coupled with the first processor interface circuitry; and

E. control logic circuitry coupled with the first processor interface circuitry, the second processor interface circuitry, the system interrupt interface circuitry, and the decode logic circuitry. Chin, column 45, lines 5-28 disclosed use of a wait state system. Chin failed to disclose the wait state circuitry.

Boutard disclosed a wait state generator for use in a processor and bus system. Boutard, Figure 27. It would have been obvious to one of ordinary skill in the art at the time of invention to use the Boutard wait state circuitry with the Chin multiprocessor system in order to allow the controllers in the Chin system to synchronize properly. Chin, column 45, lines 5-28.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2445

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. Swearingen whose telephone number is (571)272-3921. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on 571-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2445

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey R. Swearingen
Examiner
Art Unit 2445

/J. R. S./
Examiner, Art Unit 2445

/VIVEK SRIVASTAVA/
Supervisory Patent Examiner, Art Unit 2445